A DIGITAL INTEGRATED CIRCUIT TESTER

By

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A special thanks goes to Mr. Eric Strand for assembling the unit.

The schematic drawings were done by M. C. Goebel. S. J. Holland did the illustration in Figure 1. B. Cobbs did the typing.

TABLE OF CONTENTS

LIST OF FIGURES

I. Introduction.

After the introduction of an undergraduate digital systems laboratory (Electrical Engineering 249) at the University of Illinois, a need arose for a digital integrated circuit tester. The reason for this was that many times when a student had trouble, he had no easy way of knowing whether his wiring, his design, or one of his integrated circuits was at fault. The work described here was undertaken to give the student a simple way of checking his integrated circuits.

An illustration of the integrated circuit tester is presented in Figure 1. A separate printed circuit card has been programmed for each type of integrated circuit (I.C.) that is to be tested. This allows the tester itself a more general utility. Printed circuit cards have been programmed for the DTL (Diode-Transistor Logic) integrated circuit types:

MC846	Quad 2 input NAND
MC862	Triple 3 input NAND
MC858	Quad 2 input NAND power gate
MC834	Hex Inverter
MC845	Clocked Flip Flop
MC853	Dual JK Flip Flop

Cards for other circuit types may easily be programmed.

To test an I.C. (say, an MC862), the student slides the appropriate card (the one labelled MC862) into the printed circuit card holder. He then inserts his questionable I.C. into the I.C. socket on the card and pushes the test or "indicate" button. If the green light lights up, the I.C. is good. If the red light lights up, the I.C. is bad and the student must replace it.

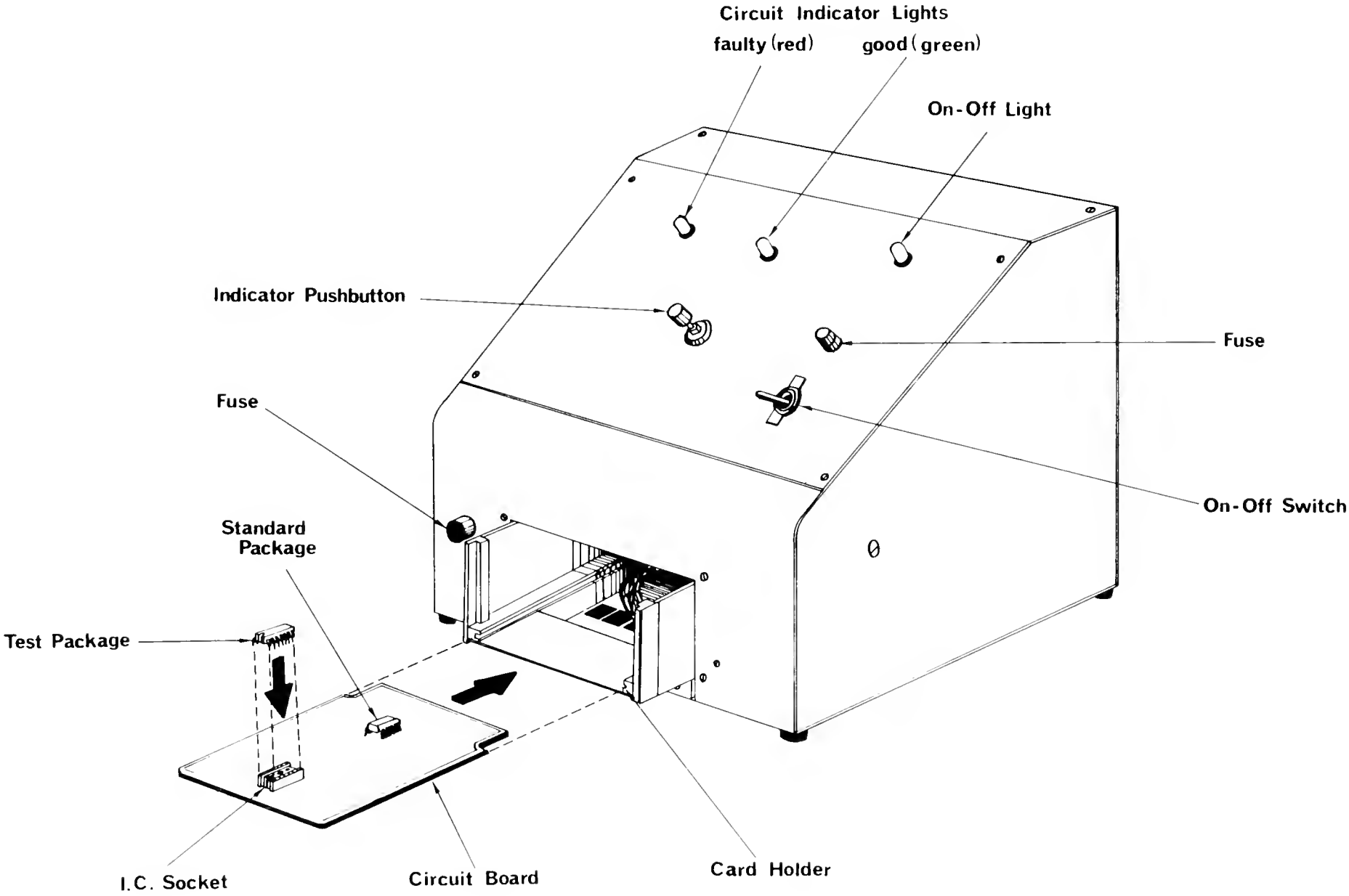


Figure 1. The Digital Integrated Circuit Tester.

II. The Design Philosophy

In the early stages of design, it was decided that the tester should be simple, versatile, fast, and reliable. A machine was desired that could reliably test most DTL integrated circuits with an immediate verdict appearing with the simple push of a button. A time deadline of four months of half-time work for the design and PCB (Printed Circuit Board) layout work imposed a further restriction.

Several different preliminary schemes were developed for testing digital integrated circuits. Of these, it was felt that only one satisfied all of the above constraints. This used a comparison scheme. In this scheme a sequence of bit patterns is administered to a standard package (which is permanently mounted on a test PCB) and to a test package such that all possible input combinations are examined. The resulting output sequences of bit patterns are compared and if they differ, a flag (a "faulty package" flip flop) is set. Caution must be exercised in setting the flag. Should the delay of a test package differ substantially from that of the standard package, a direct comparison would erroneously set the flag. Use of a delayed strobe circumvents this problem.

Testing the master-slave flip flops presents another problem. The data inputs of these devices are locked out as soon as the clock goes high and the outputs change state when the clock goes low. This being the case, a flip flop clock is required that goes high briefly after each change in input data bit pattern. After the flip flop clock has gone low, but before the data inputs have changed, the outputs of the standard and test packages must be compared. If they differ, the flag must be set. Use of a delayed strobe is again called for.

To provide a flip flop clock, a strobe, and a counter clock, a five-place ring counter with the output timing characteristics shown in Figure 2 is used. Output C_3 triggers a change in input bit pattern, B_0 being the lowest order input bit. After a one count delay, output C_0 is used as a flip flop clock (if needed). After another one count delay, output C_2 is used as a strobe. The flag is set only if the standard and test packages' outputs differ at some time while the strobe signal is high. This flag can only be reset by restarting the test. After another one count delay, the input bit pattern changes, and the cycle begins again.

The sequence of bit patterns used for data input is that of a standard ripple counter. This was used because of its simplicity.

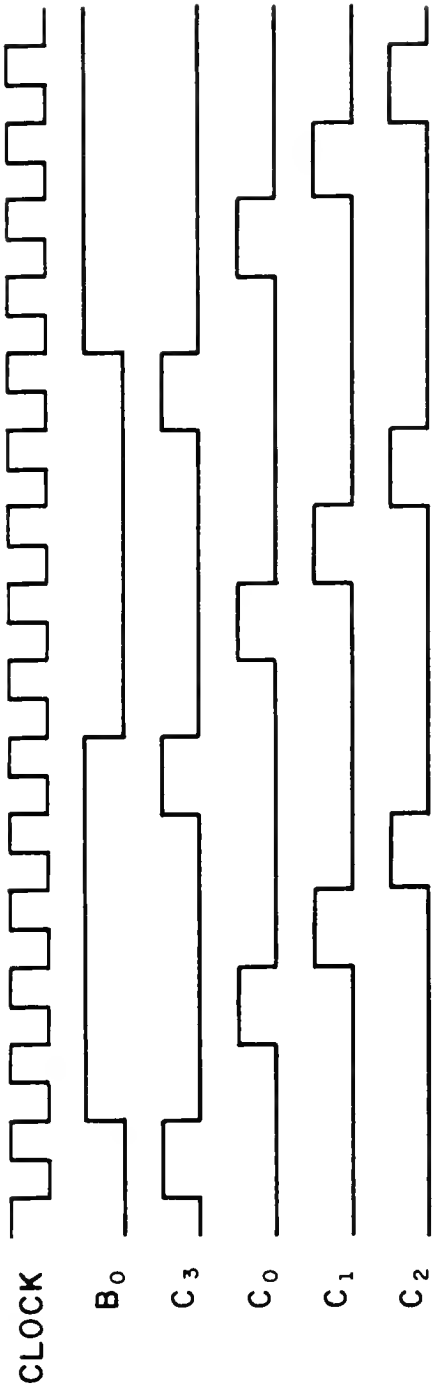


Figure 2. Waveform Timing Relationships.

III. The Circuitry.

The system diagram is shown in Figure 3. The astable multivibrator clocks the five-place ring counter. Outputs of the ring counter act as ripple counter clock, flip flop clock, and strobe as was described in the last section. Output C_3 of the ring counter clocks the 12-bit ripple counter. Only 10 bits of the ripple counter are available. Between four and nine bits of the ripple counter are used, depending upon the device being tested. These bits are used as inputs to both the standard package and the test package. Buffer inverters are used to make certain that a bad gate in the test package does not affect the input to the standard package.

The outputs from the standard package are then compared with the respective outputs from the test package using Exclusive-OR gates. The Exclusive-OR outputs are ORed when the strobe signal is high. The strobe signal becomes available only when the test button is depressed. A "de-bounce" circuit provides a test signal free of "contact bounce" as the test button is depressed. The test button signal is used to gate the strobe, to enable the flag flip flop, to turn on one of the Good/Faulty indicator lights, and to trigger a monostable which keeps the "Good" light off for about 40ms. The time delay of the latter insures that the ripple counter will have cycled through all possible input states before a good reading is registered. Note that the packages are being tested before the test button is pushed, but that a verdict is announced only after the button has been pushed. This is to allow flip flops a chance to get "in sync" before a test readout is made.

Two power supplies are used. One supplies power to the system itself and to the standard package, and the other supplies power to the test package only. Both supplies are designed with a current foldback capability so that the

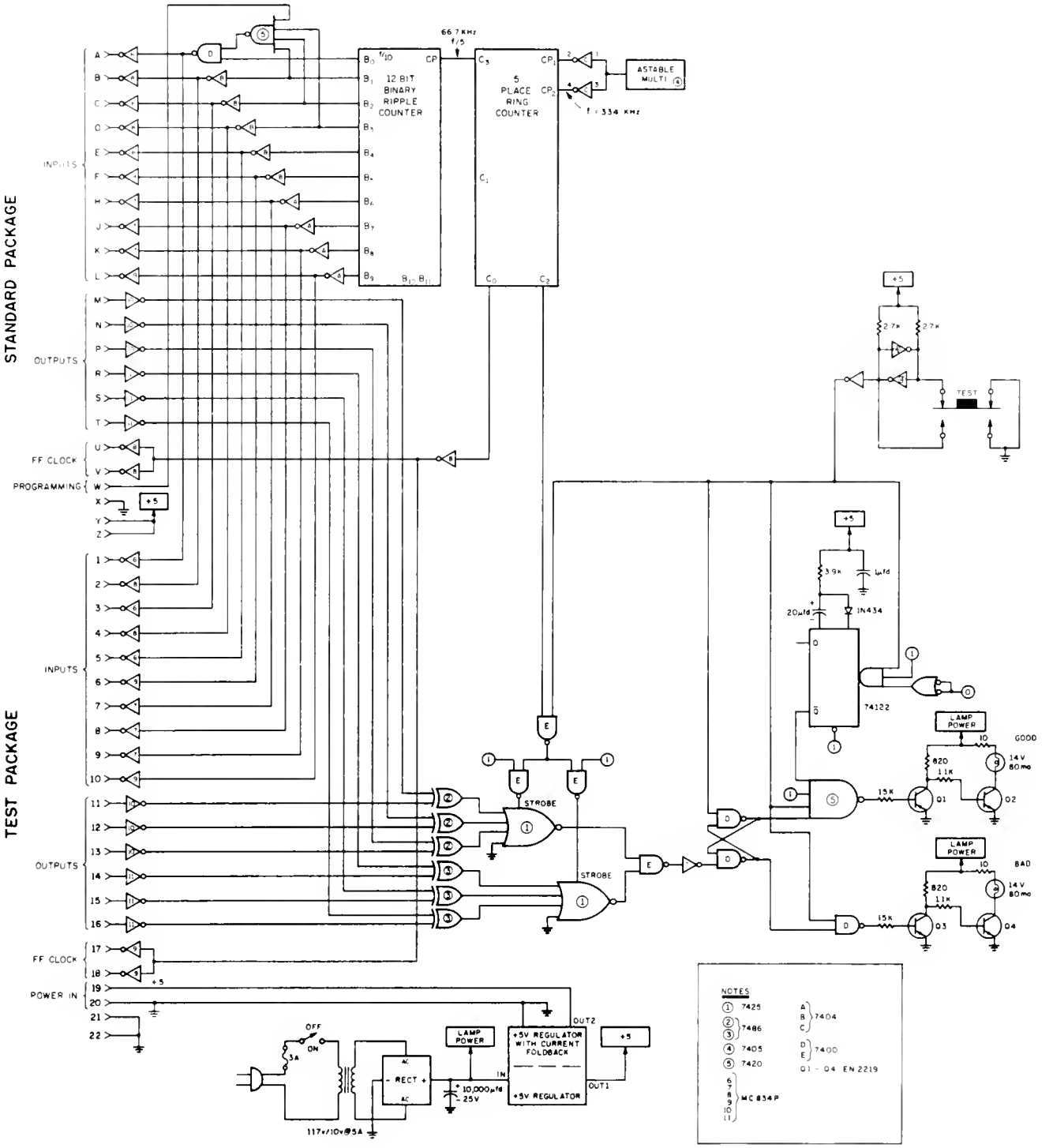


Figure 3. The System Diagram.

supplies won't be damaged under short circuit loading conditions. This feature is especially important for the test package supply.

A. Skipping the 1111 state

The data sheet for the MC845 clocked flip flop states that when the device is clocked with 1111 input, the output state is indeterminate. The circuit shown in Figure 3 and again in Figure 4 was included to eliminate any possibility of an incorrect verdict when testing the MC845. The circuit skips the 1111 state entirely as shown in Figure 4 by repeating the 1110 state twice. For circuits other than the MC845, the use of B_0 may be avoided or the programming pin may be used to eliminate the effect of the circuit. With the programming pin grounded,

$$\overline{B_0'} = \overline{B_0}.$$

B. The Astable Multivibrator

The astable multivibrator schematic diagram is shown in Figure 5. The frequency of operation is about 300 KHz. This circuit is described in [1].

C. The Five-Place Ring Counter

The circuit diagram for the five-place ring counter is shown in Figure 6. The timing relationships between the outputs are shown in Figure 2. The circuit is both self-starting and self-correcting. A complete description of the circuit operation is given in [2].

D. The Ripple Counter

The schematic diagram of the ripple counter is shown in Figure 7. The frequency of B_{11} is the frequency of the astable multivibrator divided by 20480.

E. The Power Supplies

The power supplies are shown in Figure 8. The upper supply supplies power for the tester itself and the standard package while the lower supply supplies power to the test package only. Both supplies have the capability

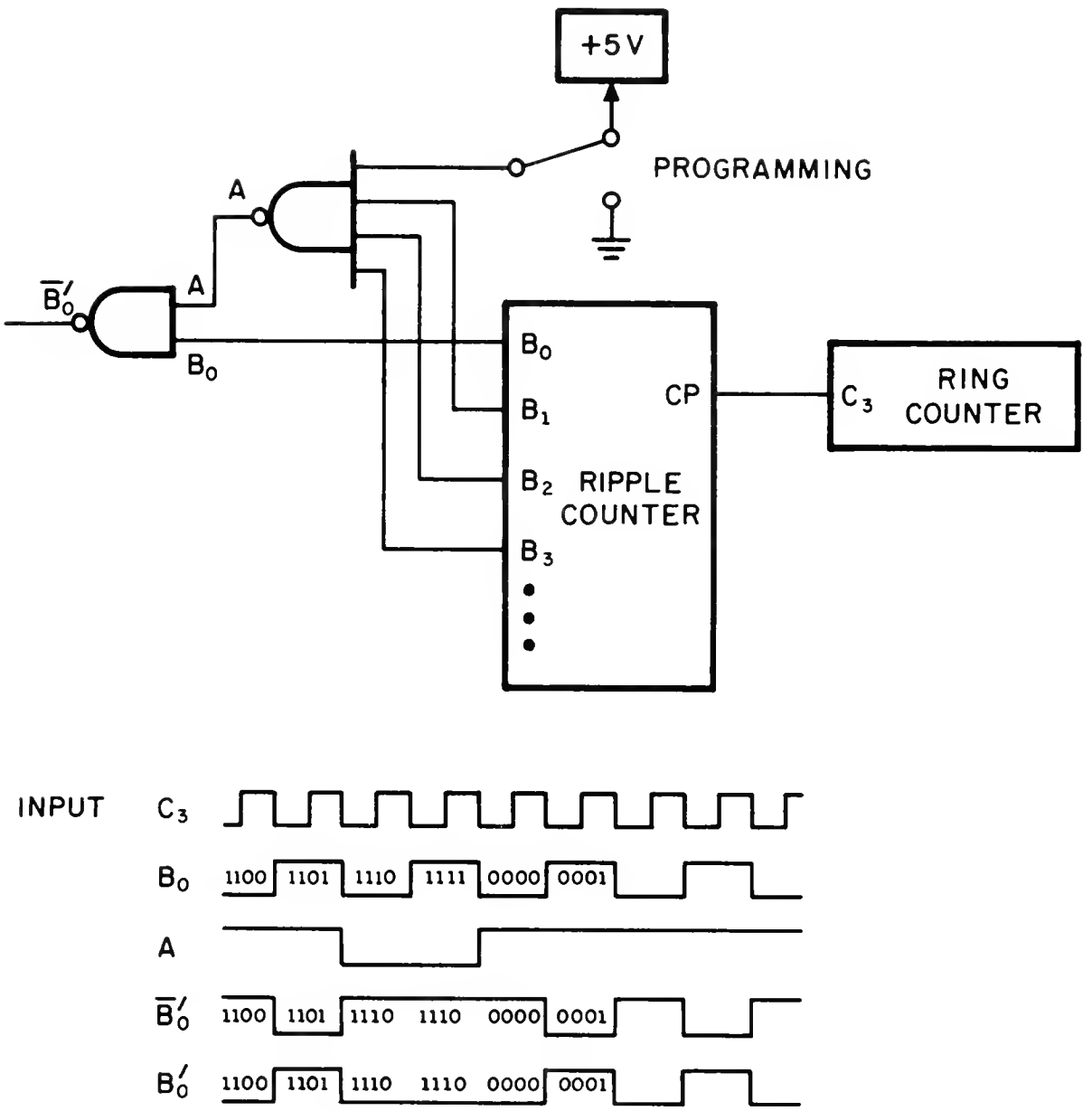


Figure 4. Circuit for Skipping 1111 State.

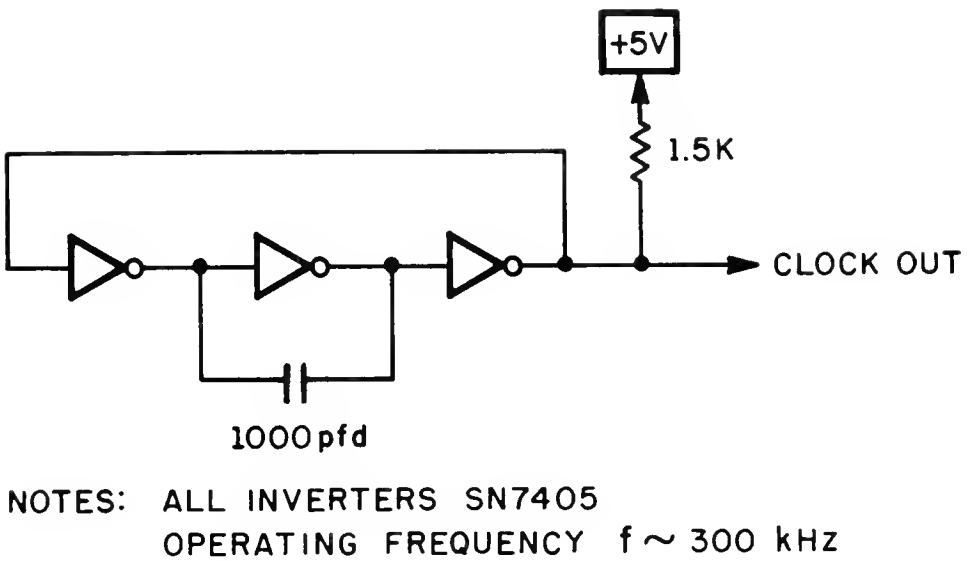


Figure 5. The Astable Multivibrator.

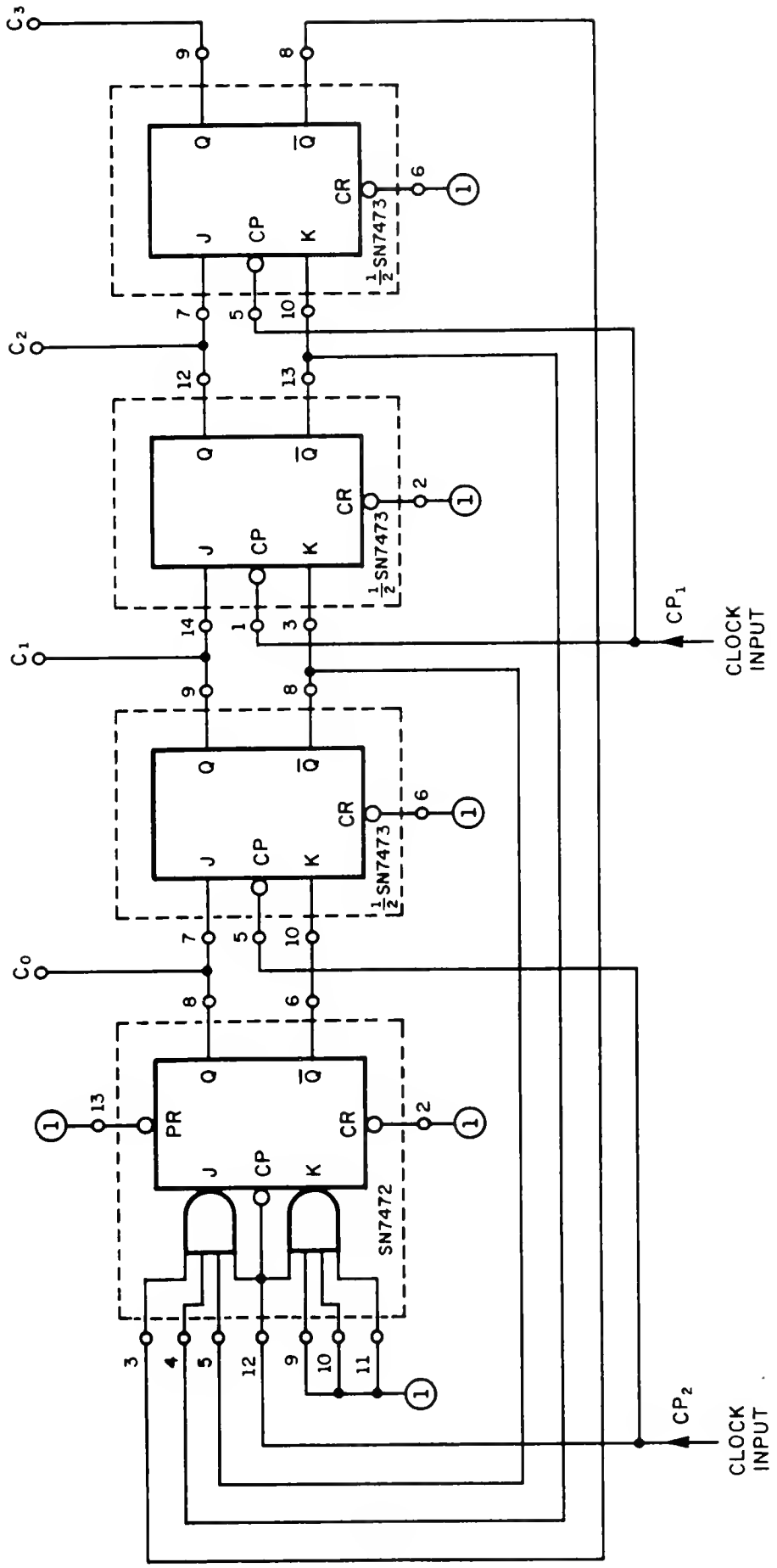


Figure 6. The Five-Place Ring Counter.

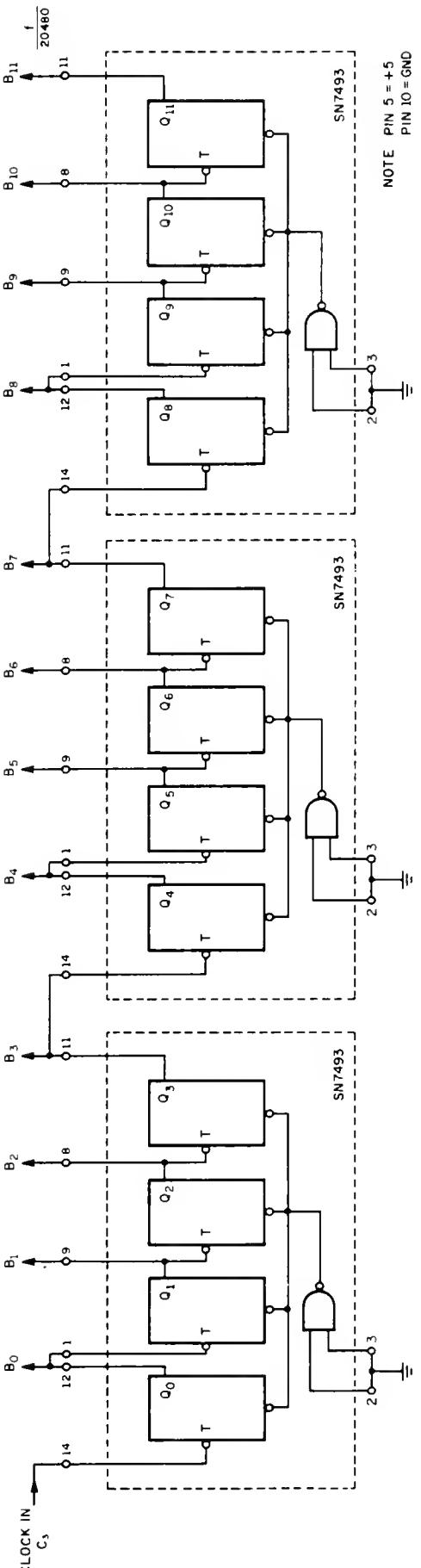
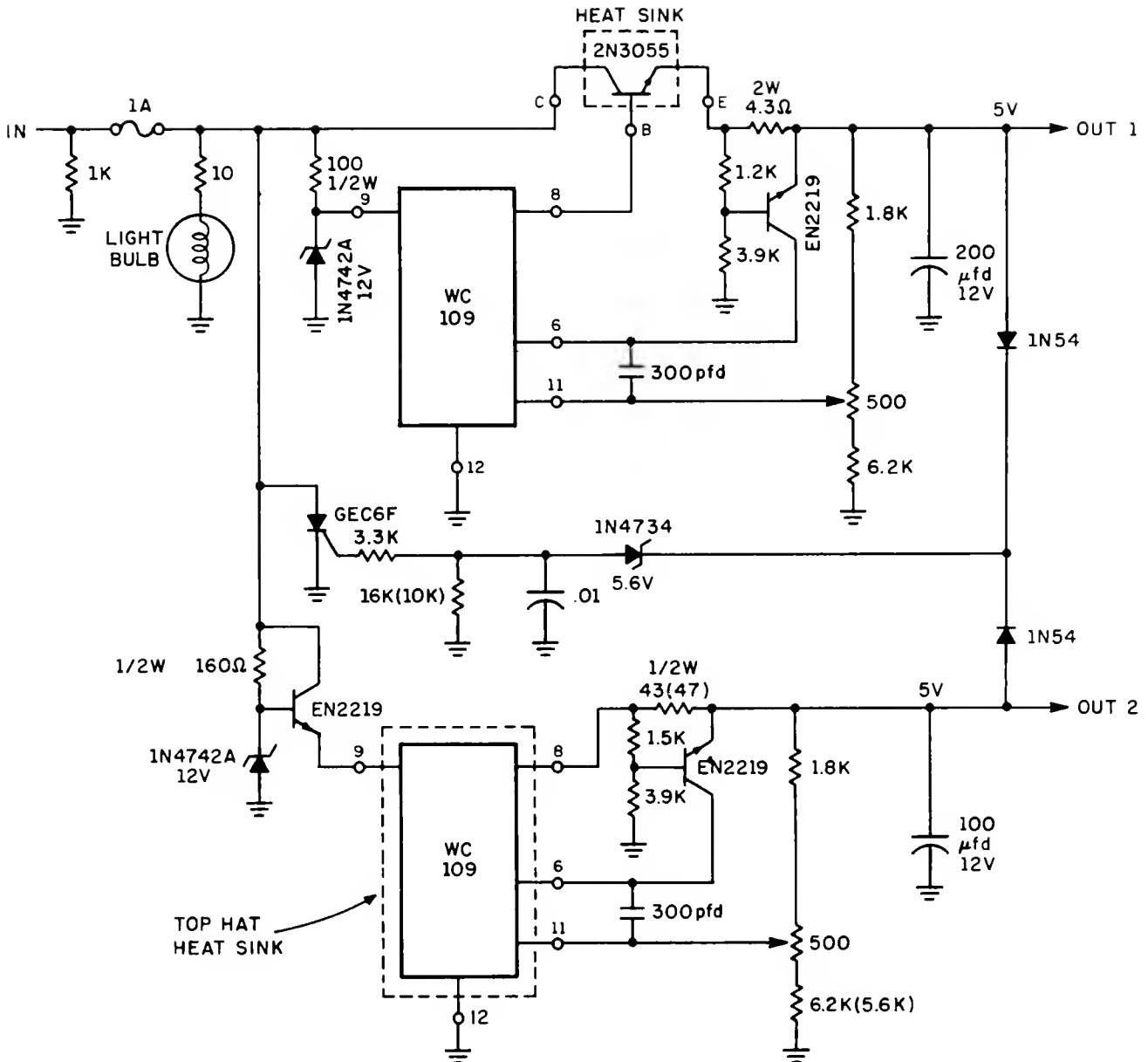


Figure 7. The 12-Bit Binary Ripple Counter.



NOTES: REGULATORS ARE WESTINGHOUSE WC 109.
USE 1A FUSES ONLY. DO NOT USE "SLOW BLOW" FUSES.
RESISTOR VALUES IN PARENTHESES REFER TO ACTUAL VALUES USED.
DESIGN DATA: (SEE MANUFACTURER'S DATA SHEET)

OUT 1: I_{MAX} = 1/2A K = .778 I_{SC} = 1/5A
OUT 2: I_{MAX} = 60mA K = .72 I_{SC} = 22mA

Figure 8. The Power Supplies.

to shut down when an output is shorted to ground. Adjustment of the output voltages is accomplished by means of the 500 Ω potentiomenters. The SCR shown provides over-voltage protection. Should either output go above about 6 volts, the SCR will fire and the 1 Ampere fuse will blow.

F. The Circuit Test Boards.

The schematic diagram of the circuit test board for the MC862 integrated circuit is shown in Figure 9. In this case, there are nine inputs and three outputs. This means that three output pins on each side of the board are not needed. These pins are all grounded to provide proper signals to the unused Exclusive-OR gates. In order that the test package may be tested under load conditions, a load resistor has been attached to each test package output. The loading resistor values used are

680 Ω	MC834, MC846, MC862
430 Ω	MC845, MC853
180 Ω	MC858 .

Note that the circuits of Figure 3 and Figure 9 are joined by the PCB connector in Figure 3 and by the PCB pins in Figure 9.

IV. The Printed Circuit Board Layouts.

The printed circuit board layout for the tester itself is shown in Figure 10. Figure 10(a) is the layout of the top of the card. The circles labelled with letters and numbers must be wired to the test card connector. The letters and numbers refer to pins on the connector. Figure 10(b) is the layout of the bottom of the card.

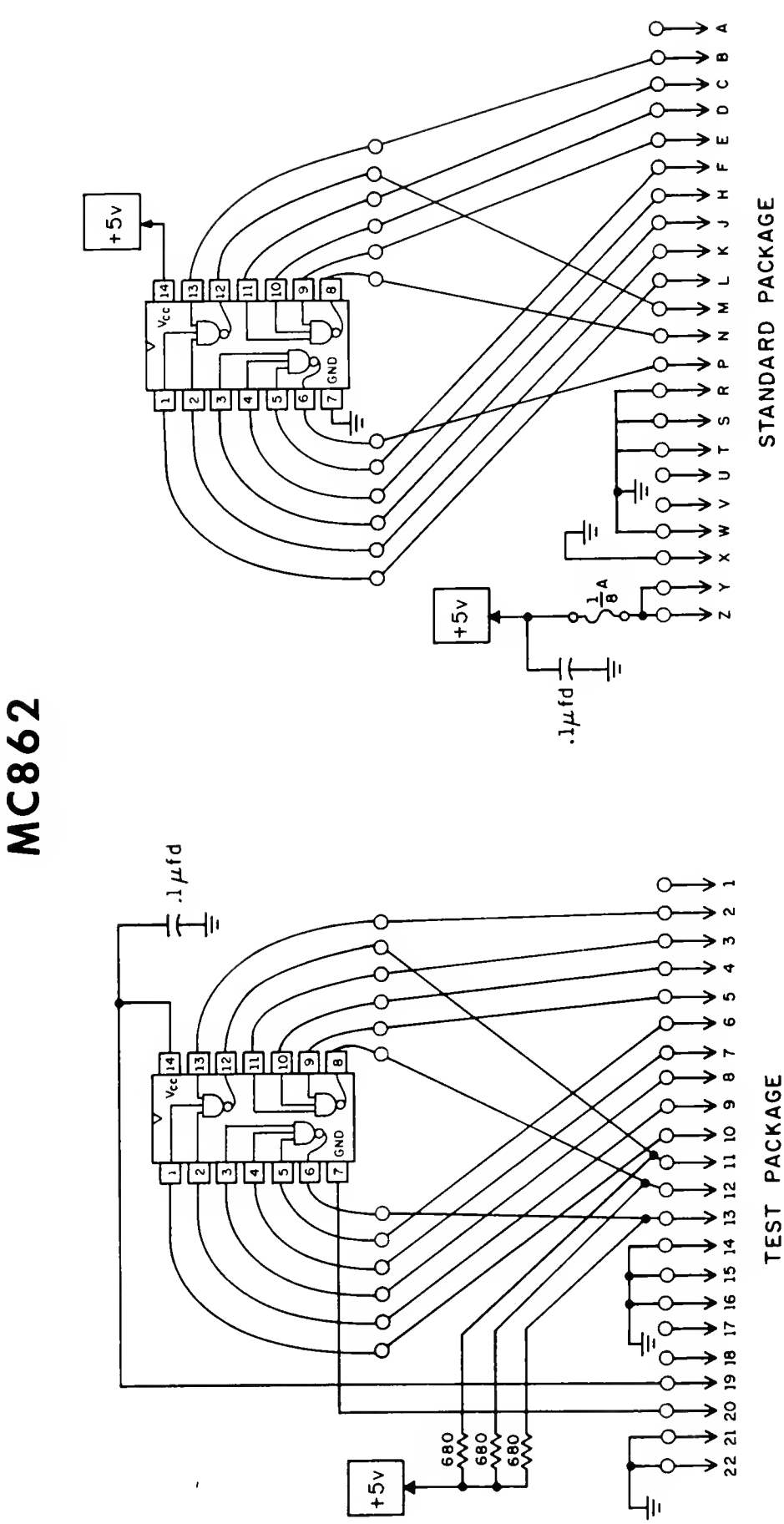


Figure 9. Example of Wiring for a Circuit Test Board.

The part locations are shown in Figure 11.

The layout for the test boards is shown in Figure 12.

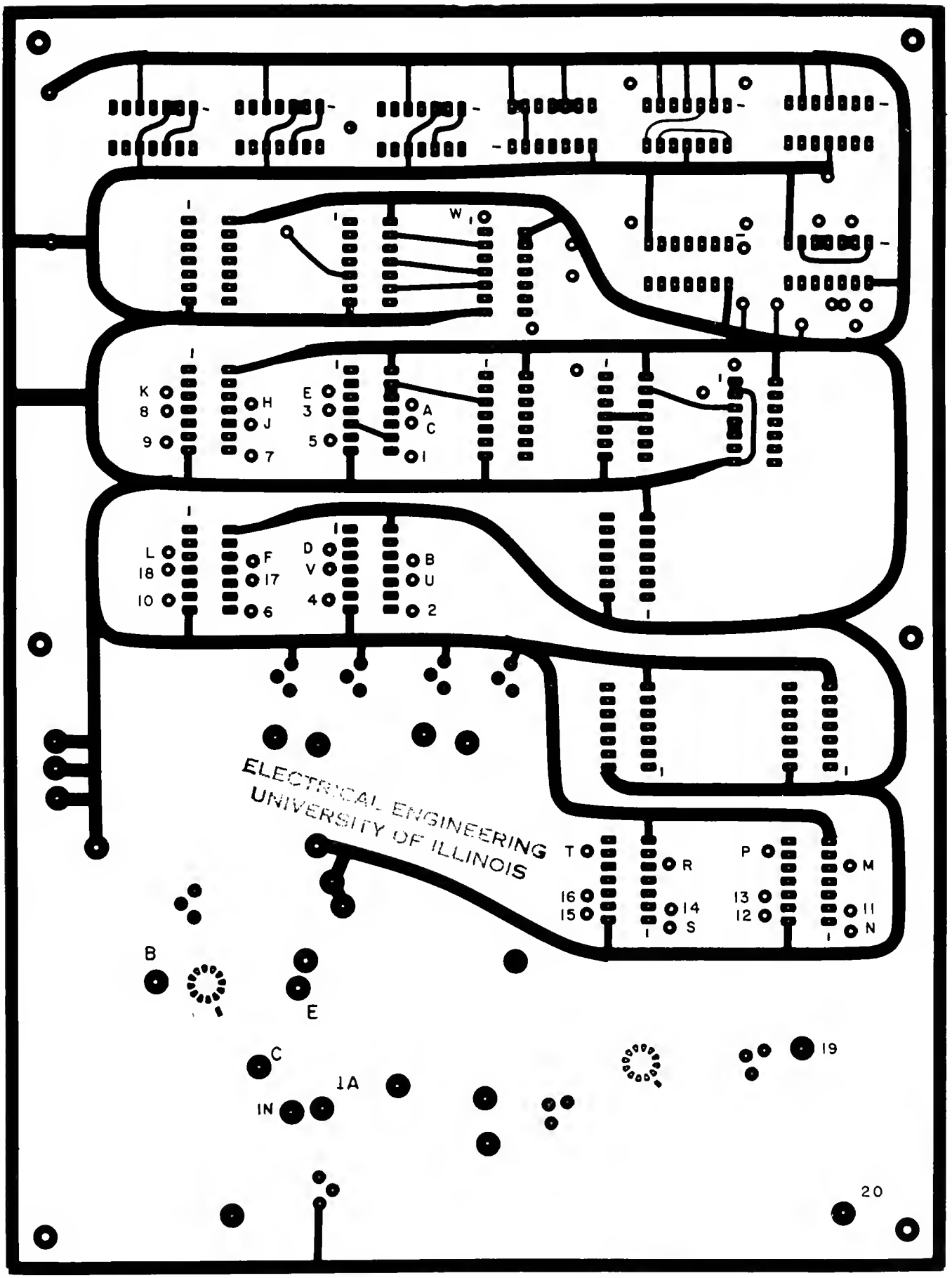


Figure 10(a). The Top Side Layout.

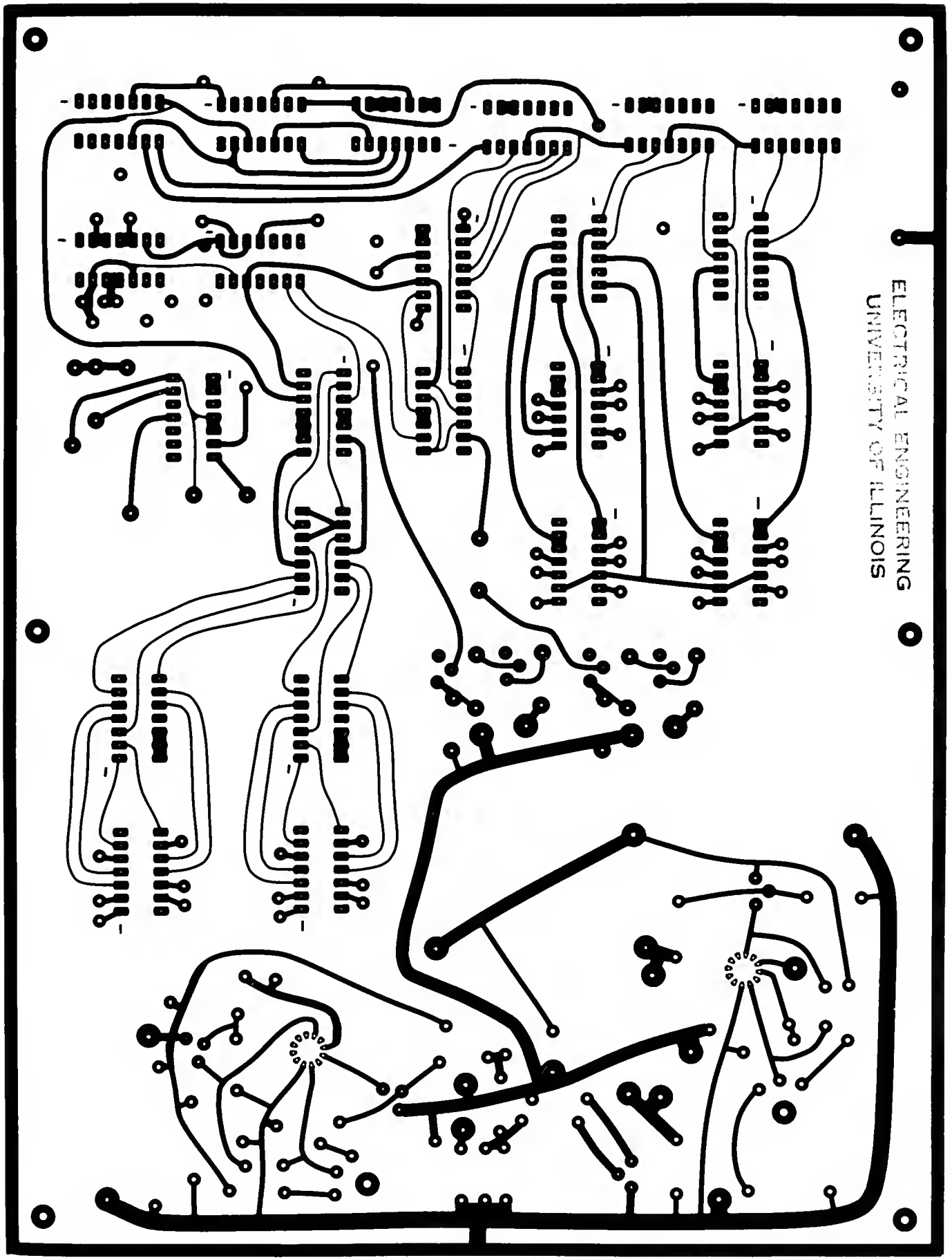


Figure 10(b). The Bottom Side Layout.

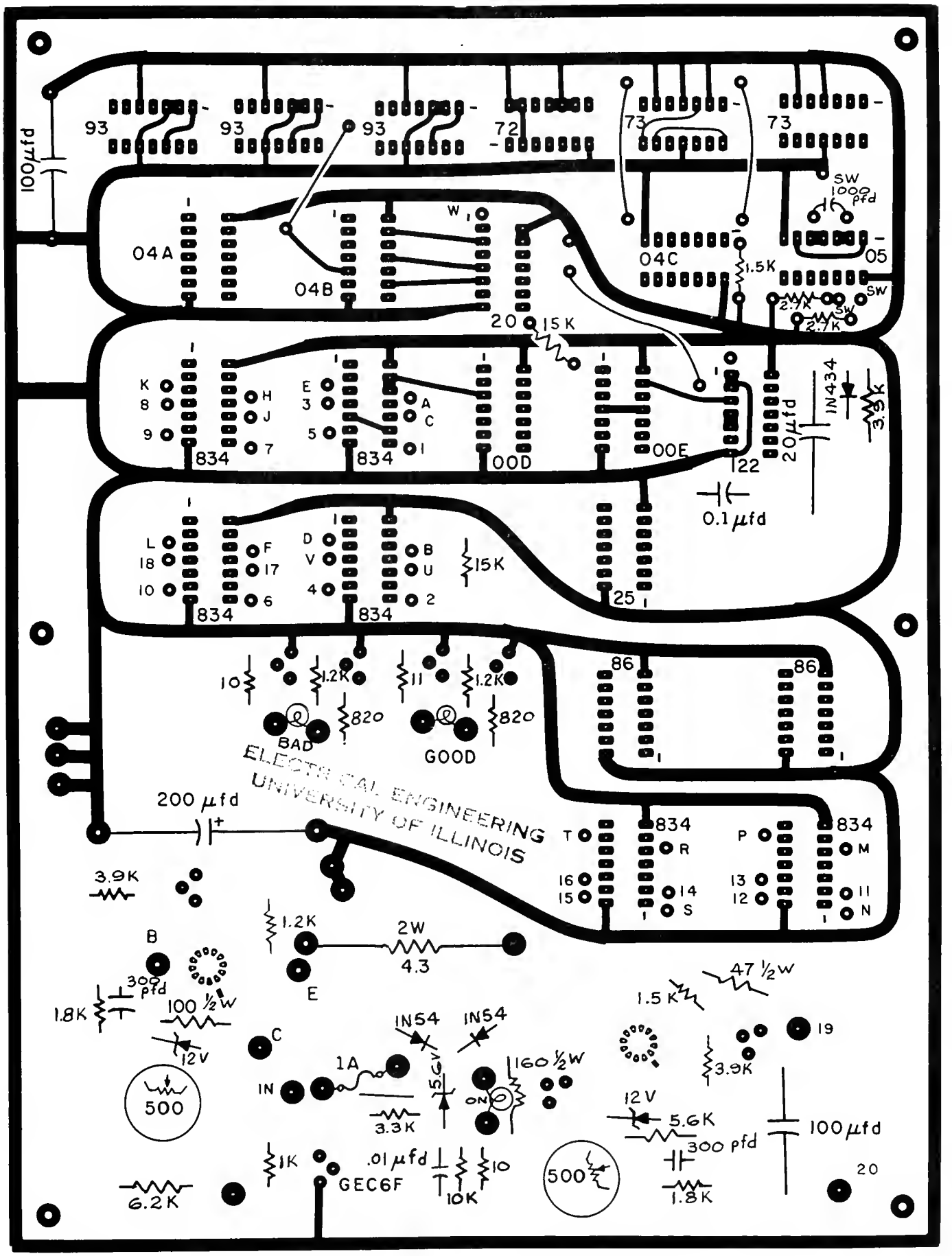


Figure 11. The Part Locations.

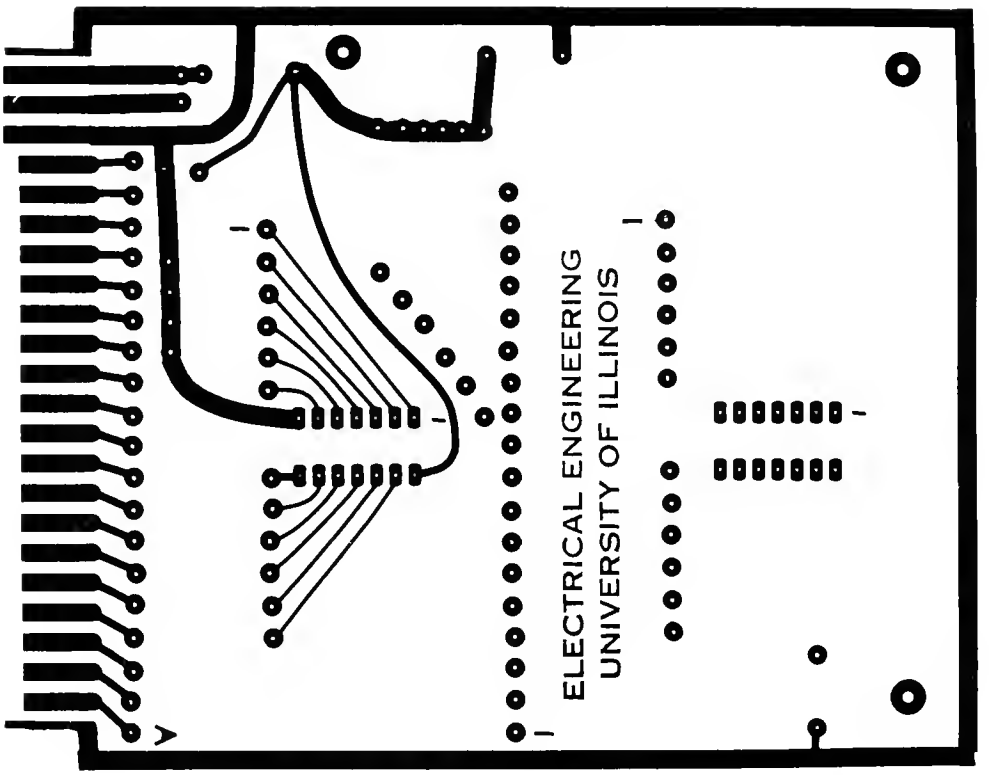


Figure 12(a). General Circuit Test Board Printed Circuit Layout. Top Side.

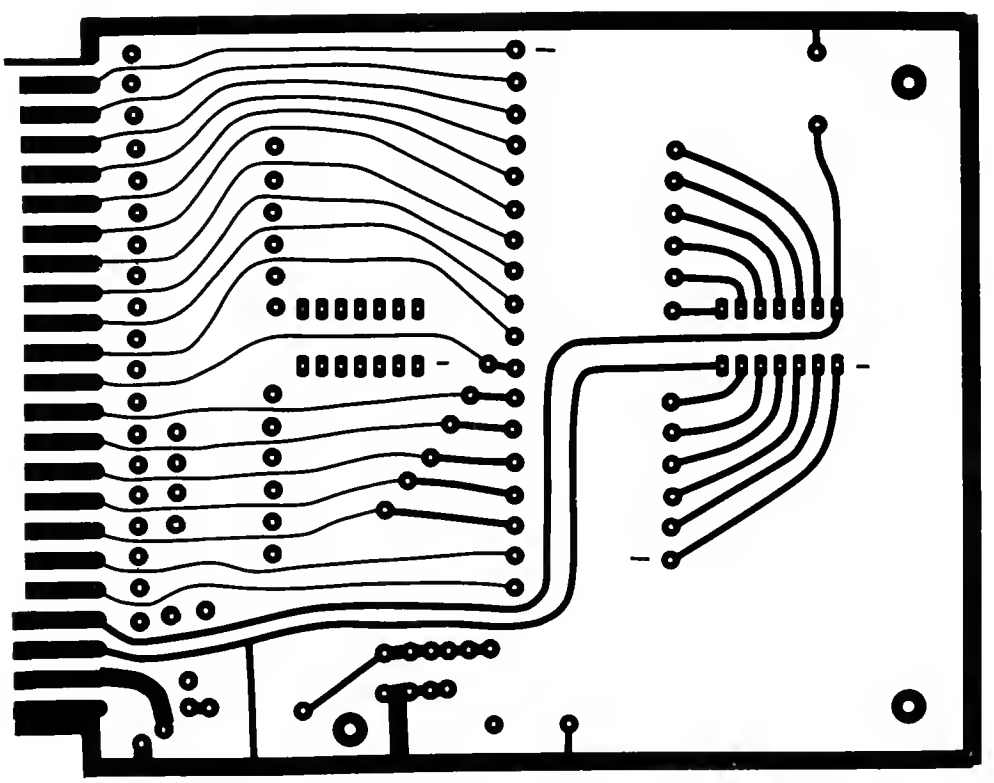


Figure 12(b). General Circuit Test Board Printed Circuit Layout. Bottom Side.

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[1] Faiman, M. "Widerange multivibrator costs just 25¢ to build", Electronics, August 2, 1971, page 59.

[2] Malmstadt, H. and Enke, C. Digital Electronics for Scientists, W. A. Benjamin, 1969, pages 272-273.